國立臺灣海洋大學一〇二學年度研究所碩士班暨碩士在職專班招生考試試題

考試科目： 電子學

系所名稱： 光電科學研究所碩士班不分組　　**※可使用計算器**

1.答案以橫式由左至右書寫。2.請依題號順序作答。

1. A conducting line on an IC chip is 1400 μm long and have a rectangular cross section 1 X 4 μm . A current of 5 mA produces a voltage drop of 100 mV across the line. Determine the electron concentration given that the electron mobility is 500 $cm^2/(V.s)$. (10%)

2. An *n-type* silicon is 1.5 mm long and has a rectangular cross section 50 X 100 μm. The donor concentration at 300 K is 5 X 10^{14} cm^{-3} and corresponds to 1 impurity atom for 10^8 silicon atoms. A steady current of 1 μA exits in the bar. Determine (a) the electron and hole concentrations; (b) the conductivity; and (c) the voltage across the bar. (Note: n_i = 1.45 X 10^{10} cm^{-3} and μ_n=1.5 x 10^3 $cm^2/(V.s)$ at 300 K) (15%)

3. Determine the output voltage v_0 in the circuit in Fig. 1 for the following values of input voltages: (a) v_1 = v_2 = 5 V; (b) v_1 = 5 V, v_2 = 0; and (c) v_1 = v_2 = 0. The silicon diodes D_1 and D_2 are identical and have R_f = 60 Ω, V_r = 0.6 V, I_s = 0, and $R_r \rightarrow \infty$. (15%)

4. An *pnp* transistor is operated with the collector-base junction reverse-biased by at least a few tenths of a voltage and with the emitter open-circuited. Determine (a) the operation mode, and (b) the values of I_C and V_{BE} at room temperature for I_{ES} = 10^{-15} A, I_{CS} = 2 X 10^{-15} A, and α_F = 0.97. (10%)

5. Design the circuit of Fig. 2. Determine the values of R_D and R_S, so that the transistor operates at I_D = 0.5 mA and V_D = +0.4 V. The NMOS transistor has V_t = 0.7 V, $\mu_n C_{OX}$ = 125 μA/V^2, L = 3 μm, and W = 150 μm. Neglect the channel-length modulation effect (i.e., assume that λ = 0). (12%)

6. For the circuit in Fig. 3 determine the values of v_1, i_1, i_2, v_O, i_L, and i_O. Also determine the power gain P_O / P_I. (Assuming the op amp to be ideal) (18%)

7. For the MOS differential pair with a common-mode voltage V_{CM} applied, as shown in Fig. 4, let V_{DD} = V_{SS} = 2.0 V, $\mu_n C_{OX}$ (W / L) = 5 mA/V^2, V_t = 0.6 V, I = 0.45 mA, and R_D = 2.0 kΩ, and neglect the channel-length modulation effect. Assume that the current source I requires a minimum voltage of 0.5 V to operate properly. (a) For V_{CM} = 0, find V_S, I_{D1}, I_{D2}, v_{D1}, and v_{D2}. (b) What is the highest permitted value of V_{CM}? (c) What is the lowest value allowed for V_{CM}? (Assuming Q_1 and Q_2 transistors are matched) (20%)

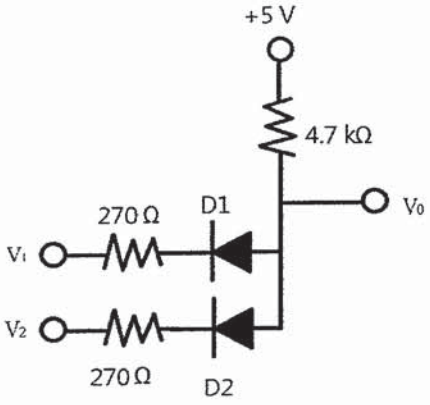

Fig. 1

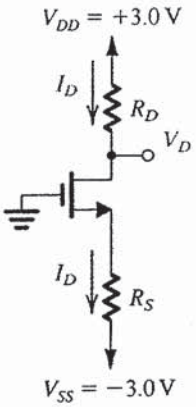

Fig. 2

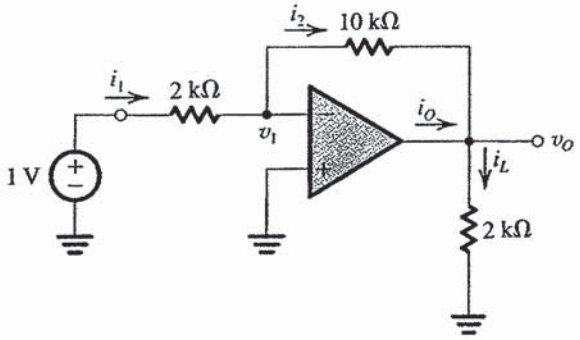

Fig. 3

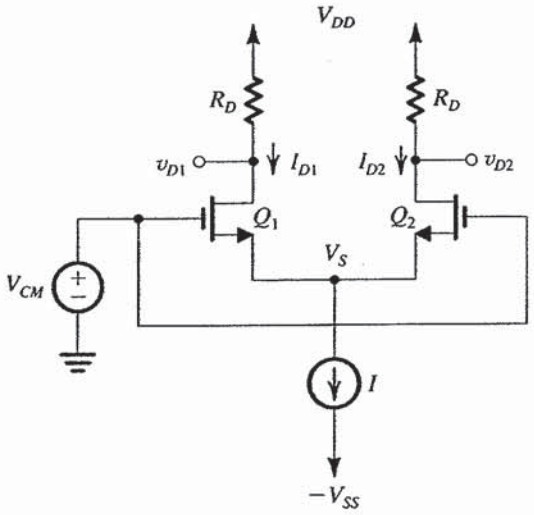

Fig.4