國立臺灣海洋大學一0二學年度研究所碩士班暨碩士在職專班招生考試試題

考試科目： 計算機結構

系所名稱： 電機工程學系碩士班資科組

1.答案以橫式由左至右書寫。2.請依題號順序作答。

1. (15%) Draw a **schematic** diagram for a 4-bit adder, using 1-bit full-adder as a basic unit

2. (15%) Explain ***sequential logic*** and ***combinational logic***. Give one example for each class.

3. (20%) Mark each of the following statements as either True or False.

   (a)___ Pipelining always increases throughput and reduces individual instruction execution time.

   (b)___ A write-through cache will not have the same miss rate as a write-back cache.

   (c)___ The Physical Address Space must be smaller than the Virtual Address Space.

   (d)___ A fully-associative cache must require more logic circuits than a direct-mapped cache of the same size.

   (e)___ Set-associative caches not necessarily always have higher hit rates than direct-mapped caches of the same size.

4. (20%) Describe **briefly** the following allocation algorithms:
   (a) First fit (b) Best fit

5 (10%) Explain the four conditions that must hold simultaneously in a system for causing a deadlock situation.

6 (20%) Consider a 4K×8 RAM chip（i.e. 4096 bytes）.
   (a) How many address lines and data lines are there in this chip ?
   (b) How many such chips do you need to construct a 64K×32 memory ?
   (c) How many address lines and data lines are there in the 64K×32 memory ?
   (d) What kind of decoder do you need to connect this 64K×32 memory ? **Draw the schematic diagram** for this 64K×32 memory construction