國立臺灣海洋大學 101 學年度研究所碩士班暨碩士在職專班入學考試試題

考試科目：電子學

系所名稱：光電科學研究所碩士班不分組　　* 可使用計算器

1.答案以橫式由左至右書寫。2.請依題號順序作答。

1. A uniform bar of n-type silicon of 5 μm length has a voltage of 1 V applied across it. If the dopant concentration $N_D=10^{17}$ cm^{-3} and the electron mobility $\mu_n=1350$ $cm^2V^{-1}s^{-1}$, find (a) the electron drift velocity, (b) the time it takes an electron to cross the 5-μm length, (c) the drift-current density, and (d) the drift current in the case the silicon bar has a cross sectional area of 0.36 μm^2. (17%)

2. Assuming that the diodes in the circuits of Fig. 1 are ideal, find the values of the labeled currents and voltages. (11%)

3. For the circuit in Fig. 2, it is required to determine the value of the voltage V_{BB} that results in the transistor operating (a) in the active mode with $V_{CE}=4$ V, (b) at the edge of saturation, (c) deep in saturation with $\beta_{forced}=10$. Assume that V_{BE} remains constant at 0.7 V and the transistor at the edge of saturation has $V_{CEsat}=0.3$ V, while the transistor deep in saturation has $V_{CEsat}=0.2$ V. The transistor β is specified to be 60. (17%)

4. The NMOS transistors in the circuit of Fig. 3 have the threshold voltage $V_t=0.5$ V, the process transconductance parameter $\mu_nC_{ox}=125$ μAV^{-2}, and channel length $L_1=L_2=1$ μm. Find the required values of gate width for each of Q_1 and Q_2, and the value of R, to obtain the voltage and current values indicated. Neglect the channel length modulation effect ($\lambda=0$). (9%)

5. The noninverting op-amp configuration shown in Fig. 4. (a) Assume that the op amp has infinite input resistance and zero output resistance. Find an expression for the feedback factor β. (b) If the open-loop gain $A=10^3$ V/V, find R_2/R_1 to obtain a closed-loop gain A_f of 10 V/V. (c) If A decrease by 30%, what is the corresponding decrease in A_f? (11%)

6. For the circuit of Fig. 5 with $V=12$ V, $R_1=20$ kΩ, $R_f=60$ kΩ, $R_2=R_5=10$ kΩ, and $R_3=R_4=4$ kΩ, find the limiting levels and the value of v_I at which the limiting levels are reached. Also determine the limiter gain and the slope of the transfer characteristic in the positive and negative limiting regions. Assume that diode voltage $V_D=0.7$ V. (20%)

7. For the CMOS class AB output stage of Fig. 6, consider the case of matched Q_1 and Q_2, and matched Q_N and Q_P. If quiescent current $I_Q=1.2$ mA in Q_N and Q_P, find (W/L) for each of Q_1, Q_2, Q_N, and Q_P so that in the quiescent state each transistor operates at an overdrive voltage of 0.2 V. Let $V_{DD}=V_{SS}=2.5$ V, the process transconductance parameter $k'_n=200$ μAV^{-2}, $k'_p=100$ μAV^{-2}, and the threshold voltage $V_{tn}=-V_{tp}=0.6$ V. Also find V_{GG}. Assume that $I_{BIAS}=0.3$ mA and neglect the channel length modulation effect ($\lambda=0$). (15%)

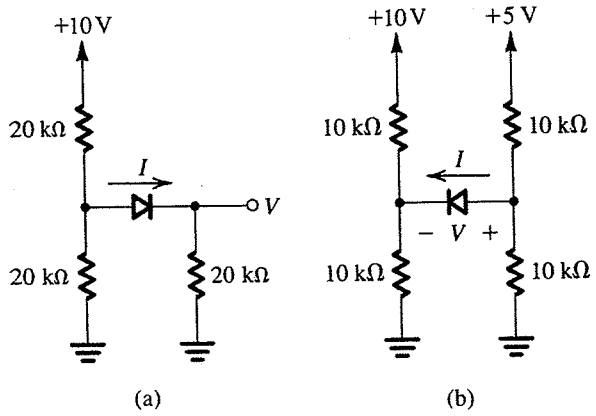

Fig. 1

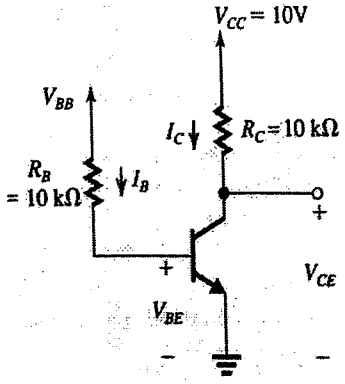

Fig. 2

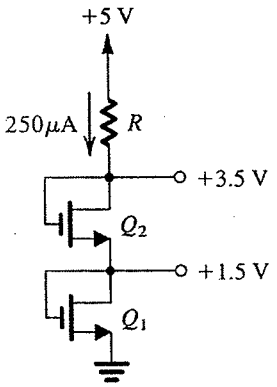

Fig. 3

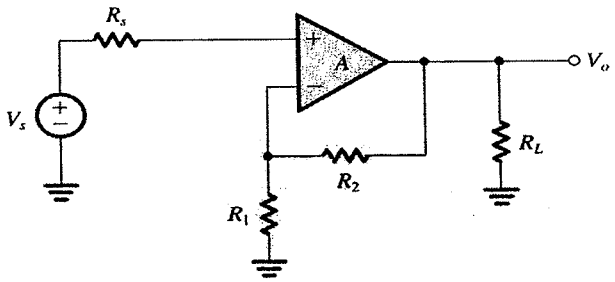

Fig. 4

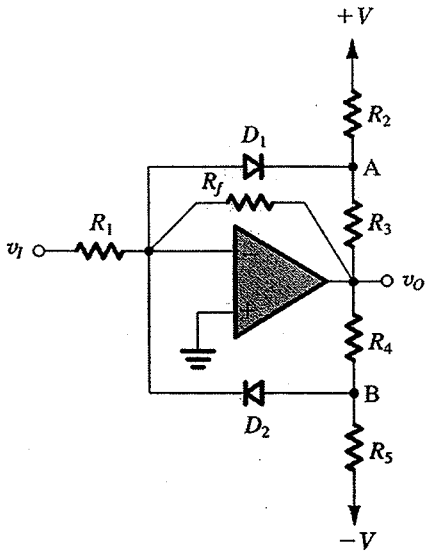

Fig. 5

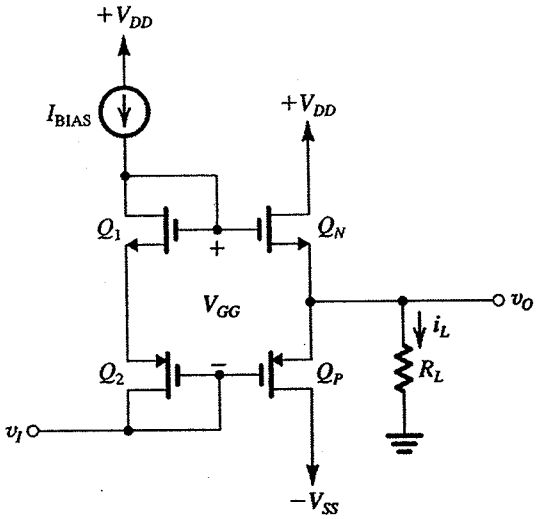

Fig. 6