國立臺灣海洋大學 100 學年度轉學生入學招生考試試題

考試科目： 電子電路

＊可使用計算機

系所名稱： 日通訊三

1.答案以橫式由左至右書寫。2.請依題號順序作答。

1. 選擇題 (單選題, 10%, 每小題兩分)

甲、Which of the following statements is wrong for an ideal voltage amplifier? (a) an infinitely high input resistance; (b) an infinitely high output resistance, and (c) an infinitely high open-circuit voltage gain.

乙、Which of the followings is NOT true for an ideal transconductance amplifier? (a) the input signal is voltage; (b) the output signal is current; (c) $R_i = \infty$; (d) $R_o = 0$.

丙、Which one is NOT true when a reverse bias is applied to a *pn* junction? (a) current flows from *n*-type to *p*-type region (b) depletion-layer width increases (c) diffusion capacitance dominates (d) breakdown may take place if the reverse voltage is too high.

丁、"Early effect" and "channel length modulation" are commonly observed in modern transistor devices. Which of the following properties is NOT caused by such effects? (a) The base width of BJT is reduced (b) The turn-on voltage of MOSFET is reduced (c) The channel of the MOSFET is pinch-off (d) The emitter current of the BJT is increased.

戊、In the follow feedback topologies, which one can decrease the input resistance and increase the output resistance? (a) series-shunt (b) series-series (c) shunt-shunt (d) shunt-series.

2. For the circuit in Figure 1, the transfer function of the basic amplifier A is $A = \dfrac{200}{1 + jf/10K}$. The feedback factor β is 0.01. Calculate the upper 3 dB frequency and the phase margin of the feedback amplifier. (You don't need to use the Bode plots.) (20%)

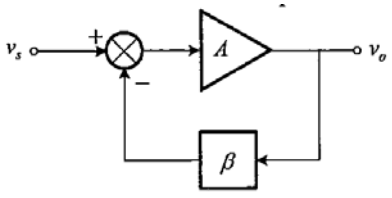

Figure 1

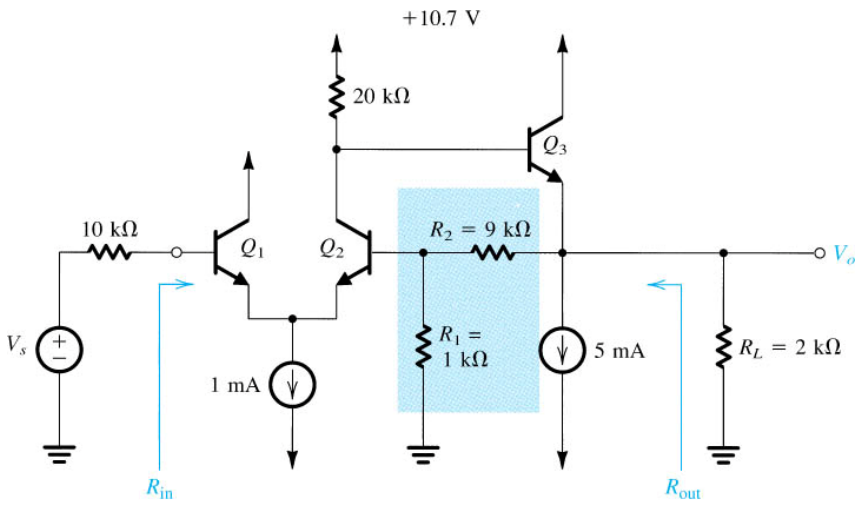

Figure 2

3. For the circuit shown in Figure 2 with series-shunt feedback topology, assume that the DC component of V_S is zero. (a) Assume β of the BJTs is very high. Find the DC operating current of each

of the three transistors and show that the DC voltage at the output is approximately zero. (5%) (b) Assume that the transistors have $\beta = 100$. Then find the values of A, β_f (feedback gain), $A_f := V_O / V_S$, R_{in}, and R_{out}. (15%)

4.The variable resistor R in Fig.1 is adjusted until it absorbs the maximum power from the circuit.

(a) Obtain the Thevenin equivalent at terminal a - b. (10%)

(b) Calculate the value of R for maximum power. (5%)

(c) Determine the maximum power absorbed by R. (5%)

5. In Fig. 2 switch 1 (S_1) is closed at t = 0, and switch 2 (S_2) is closed 4 sec. later.

Find i(t) for $t < 0$, $0 \le t < 4$, and $t \ge 4$. (20%)

6.Consider the circuit in Fig. 3. Find i_s (t). (10%)

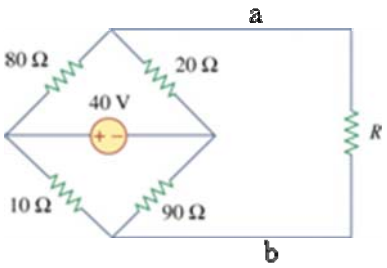

Fig.1

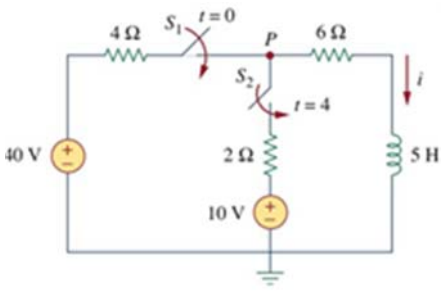

Fig.2

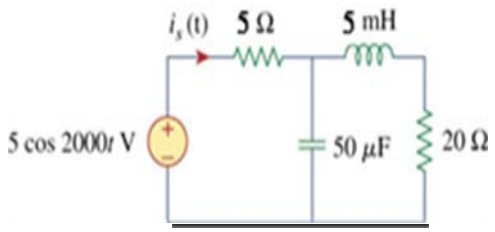

Fig.3